

IN THE CLAIMS:

All of the pending claims 1-9 and 13 are set forth below. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (previously presented), or (new). Please AMEND claim 1 and ADD claim 13 in accordance with the following:

1. (currently amended) An error detection/correction system in data transmission between a plurality of modules that are connected via buses in a controller, the system comprising:

in each of the modules,

a plurality of error detection/correction code generation circuits having a difference in at least one of an inspection bit length, an information bit length, and a correction capacity; and

a plurality of error detection/correction circuits corresponding to a respective one of the error detection/correction code generation circuits, wherein ~~the~~an error detection/correction code generation circuit and ~~the~~an error detection/correction circuit are switched over dependent upon a kind, a length, and a timing of the data to be transferred.

2. (original) The error detection/correction system according to claim 1, wherein the error detection/correction system switches over between error detection/correction codes to be used dependent upon on a phase of transmitting an address, a command, and data.

3. (original) The error detection/correction system according to claim 1, wherein the error detection/correction system switches over error detection/correction codes to be used dependent upon whether at a time of single access or at a time of burst access.

4. (original) The error detection/correction system according to claim 1, wherein the error detection/correction system switches over between error detection/correction codes to be used, dependent upon a data quantity to be transferred.

5. (previously presented) A controller in which a plurality of modules that adopt the error detection/correction system according to claim 1 are connected via buses.

6. (previously presented) The controller according to claim 5, wherein the controller comprises a serial transfer module that connects a plurality buses connected with the plurality of modules, by means of a serial transmission line, and

a plurality of error detection/correction code generation circuits having a difference in at least one of an inspection bit length, an information bit length, and a correction capacity, and error detection/correction circuits corresponding to the error detection/correction code generation circuits are built into the serial transfer module, and the error detection/correction system is used for the serial transfer.

7. (previously presented) A controller in which a plurality of modules that adopt the error detection/correction system according to claim 2 are connected via buses.

8. (previously presented) A controller in which a plurality of modules that adopt the error detection/correction system according to claim 3 are connected via buses.

9. (previously presented) A controller in which a plurality of modules that adopt the error detection/correction system according to claim 4 are connected via buses.

10–12. (cancelled)

13. (new) An error detection/correction system, comprising:
a plurality of modules connected via buses to transmit data, each of the modules including,
a plurality of error detection/correction code generation circuits and a plurality of error detection/correction circuits corresponding to a respective one of the error detection/correction code generation circuits, wherein an error detection/correction code generation circuit and an error detection/correction circuit are switched over dependent upon a kind, a length, and a timing of the data to be transferred.